IN THE CLAIMS:

Please amend the claims to read as follows:

1. (Currently Amended) A circuit comprising

a first three-to-two reducer;

a second three-to-two reducer directly connected to the first three-to-two reducer;

a first clock input connected to the first three-to-two reducer to receive a first clock signal; and

a second clock input connected to the second three-to-two reducer to receive a second clock signal that is delayed from the first clock signal wherein the delay between the first clock signal and the second signal is ~~caused by~~ approximately the delay of an inverter circuit with a fanout of ~~at least~~ 2.

2-4. (Cancelled).

5. (Previously Presented) The circuit of claim 1, wherein the circuit further comprises two set-reset latches to convert the outputs of the second three-to-two reducer to static logic.

6. (Previously Presented) The circuit of claim 1, wherein the first and second three-to-two reducer both comprise a symmetric carry generate gate.

7. (Original) The circuit of claim 6, wherein the symmetric carry generate gates have a first evaluation block of transistors and a second evaluation block of

transistors, wherein the first evaluation block and second evaluation block each have the same number of transistors.

8. (Original) The circuit of claim 7, wherein the symmetric carry generate gates have six data inputs, and wherein the gate of each of the transistors in both the first evaluation block and the second evaluation block is connected to one of the six data inputs.

9. (Previously Presented) The circuit of claim 7, wherein the first evaluation block comprises a plurality of transistors connected in a parallel relationship to each other and a plurality of transistors connected in a serial relationship to each other, wherein the second evaluation block comprises a plurality of transistors connected in a parallel relationship to each other and a plurality of transistors connected in a serial relationship to each other, and wherein the second evaluation block has the same number of transistors in said parallel relationship as the first evaluation block and the same number of transistors in said serial relationship as the first evaluation block.

10. (Previously Presented) A circuit comprising:

a first differential domino three-to-two reducer having three differential inputs and two differential outputs, wherein the first differential domino three-to-two reducer has an input to receive a first clock signal; and

a second differential domino three-to-two reducer having three differential inputs and two differential outputs, wherein one of the differential inputs of the second differential three-to-two reducer is connected to a differential output of the first differential three-to-two reducer, wherein the second differential domino three-to-two reducer has an input to receive a different clock signal.

11. (Previously Presented) The circuit of claim 10, wherein there are no static stages between the first and second differential domino three-to-two reducers.

12. (Previously Presented) The circuit of claim 10, wherein the first differential three-to-two reducer comprises:

a differential exclusive-OR (XOR) gate having three differential inputs and a differential output; and

a differential carry generate gate having three differential inputs and a differential output.

13. (Previously Presented) The circuit of claim 12, wherein the three differential inputs to the carry generate gate comprise three true inputs and three complement inputs, and wherein the Miller coupling for the true inputs is equal to the Miller coupling for the complement inputs.

14. (Previously Presented) The circuit of claim 13, wherein the differential output of the carry generate gate comprises a true output and a complement output, and wherein the output drive strength for the true output is the same as the output drive strength for the complement output.

15. (Previously Presented) The circuit of claim 12, wherein the load for the true inputs to the carry generate gate is the same as the load for the complement inputs, wherein the pull down strength for the true output is the same as the pull down strength for the complement output, and wherein the pull down strength for the true inputs is the same as the pull down strength for the complement inputs.

16.-20 (Cancelled)

21. (Previously Presented) A method comprising:

receiving three pair of true and complement data bits at a first differential domino three-to-two reducer;

outputing a first pair of true and complement sum bits from the first three-to-two reducer to a second differential domino three-to-two reducer during the evaluation phase of a first clock;

receiving a fourth pair of true and complement data bits at the second differential domino reducer; and

outputting a second pair of true and complement sum bits and a pair of true and complement carry output bits output during the evaluation phase of a second clock that is delayed from the first clock.

22. (Previously Presented) The method of claim 21, wherein the first pair of true and complement sum bits are outputted directly to the second three-to-two reducer from the first three-to-two reducer.

23. (Previously Presented) The method of claim 22, wherein providing the first true and complement sum bits to the second three-to-two reducer comprises:

outputting the first true and complement sum bits to an exclusive-or (XOR) gate; and

outputting the first true and complement sum bits to a symmetric carry generate gate.

24. (Previously Presented) The method of claim 21, wherein the method further comprises:

receiving the second true and complement sum bits at a first latch;

outputting a true sum output from the first latch;

receiving the true and complement carry output bits at a second latch; and

outputting a complement sum output from the second latch.

25. (Previously Presented) A circuit comprising a domino four-to-two reducer, wherein the four-to-two reducer comprises:

a first three-to-two reducer that comprises a first logic gate, the first logic gate comprising a first evaluation block and a plurality of outputs, the first evaluation block comprising N-channel metal-oxide semiconductor transistors;

a second three-to-two reducer that comprises a second logic gate, the second logic gate comprising a second evaluation block and a plurality of inputs that are directly connected to the outputs of the first logic gate, the second evaluation block comprising N-channel metal-oxide semiconductor transistors;

a first clock input connected to the first three-to-two reducer to receive a first clock signal; and

a second clock input connected to the second three-to-two reducer to receive a second clock signal that is delayed from the first clock signal.

26. (Cancelled)

27. (Currently Amended) The circuit of claim 25, wherein the delay between the first clock signal and the second clock signal is approximately the delay of an inverter with a fanout of 2.

28. (Previously Presented) The circuit of claim 25, wherein the four-to-two reducer further comprises two set-reset latches to convert the outputs of the second three-to-two reducer to static logic.

29. (Previously Presented) The circuit of claim 25, wherein the first evaluation block and second evaluation block each have the same number of transistors.

30. (Previously Presented) The circuit of claim 25, wherein the first logic gate and second logic gate are both symmetric carry generate gates.

31. (Previously Presented) The circuit of claim 30, wherein the symmetric carry generate gates have six data inputs, and wherein the gate of each of the

transistors in both the first evaluation block and the second evaluation block is connected to one of the six data inputs.

32. (Previously Presented) The circuit of claim 25, wherein the first evaluation block comprises a plurality of transistors connected in a parallel relationship to each other and a plurality of transistors connected in a serial relationship to each other, wherein the second evaluation block comprises a plurality of transistors connected in a parallel relationship to each other and a plurality of transistors connected in a serial relationship to each other, and wherein the second evaluation block has the same number of transistors in said parallel relationship as the first evaluation block and the same number of transistors in said serial relationship as the first evaluation block.

33. (Previously Presented) A circuit comprising:

a first differential domino three-to-two reducer having three differential inputs and two differential outputs; and

a second differential domino three-to-two reducer having three differential inputs and two differential outputs, wherein one of the differential inputs of the second differential three-to-two reducer is connected to a differential output of the first differential three-to-two reducer, and wherein there are no static stages between the first and second differential domino three-to-two reducers, wherein the first differential domino three-to-two reducer has an input to receive a first clock signal and the second differential domino three-to-two reducer has an input to receive a different clock signal.

34. (Cancelled).

35. (Previously Presented) The circuit of claim 33, wherein the first differential three-to-two reducer comprises:

a differential exclusive-OR (XOR) gate having three differential inputs and a differential output; and

a differential carry generate gate having three differential inputs and a differential output.

36. (Previously Presented) The circuit of claim 35, wherein the three differential inputs to the carry generate gate comprise three true inputs and three complement inputs, and wherein the Miller coupling for the true inputs is equal to the Miller coupling for the complement inputs.

37. (Previously Presented) The circuit of claim 36, wherein the differential output of the carry generate gate comprises a true output and a complement output, and wherein the output drive strength for the true output is the same as the output drive strength for the complement output.

38. (Previously Presented) The circuit of claim 35, wherein the load for the true inputs to the carry generate gate is the same as the load for the complement inputs, wherein the pull down strength for the true output is the same as the pull down strength for the complement output, and wherein the pull down strength for the true inputs is the same as the pull down strength for the complement inputs.